ABSTRACT OF THE DISCLOSURE

A system and method for building a test case operable to test a circuit design, the test case including a summary of instructions. In one embodiment, an instruction generation engine generates a set of instructions of which at least one instruction includes a temporarily uncommitted value. A first summary generation engine portion generates an interfaceable enumeration of the set of instructions wherein each of the temporarily uncommitted values is denoted by an uncommitted reference. A second summary generation engine portion resolves the respective values of the uncommitted references and generates an interfaceable listing of the uncommitted references and their the respective values. The set of instructions and the interfaceable listing of the resolved uncommitted references may be arranged to form the test case.